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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/788,492	03/01/2004	Nobuaki Hashimoto	118876	9029

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EXAMINER	
RICHARDS, N DREW	
ART UNIT	PAPER NUMBER
2815	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	01/05/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/788,492	HASHIMOTO, NOBUAKI	
	Examiner	Art Unit	
	N. Drew Richards	2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *04 December 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-12,17 and 18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-12,17 and 18* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *01 March 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 112

1. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. Claims 3 and 11 recite the limitation "the electrode" in line 3. There is insufficient antecedent basis for this limitation in the claim.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

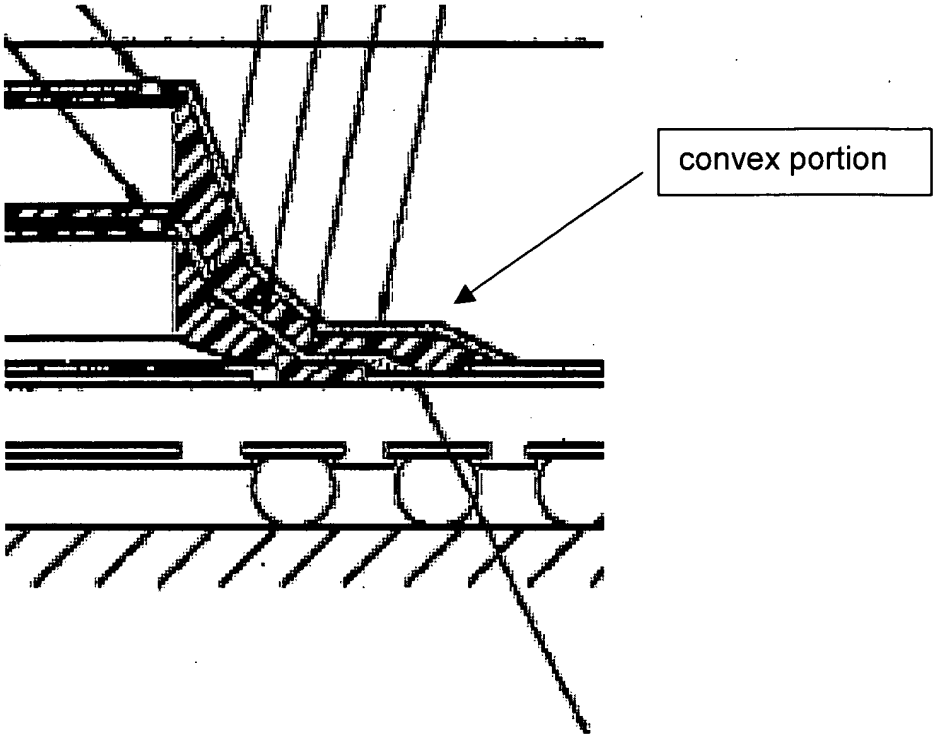
4. Claims 1, 3-5, 11, 12, 17 and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nakanishi (US 6,756,252 B2) in view of Ling et al. (USPAT 6,445,069 B1).

With regard to claim 1, Nakanishi teaches an electronic device in figure 14A comprising:

- a substrate 84 on which an interconnect pattern 100 is formed;
- a chip component 10b having a base material and having a first surface (top surface) on which a pad (not labeled in figure 14A, however column 7 lines 63-64 indicate that the embodiment of figure 14A is similar to that described previously,

thus similar to that of figure 10 which shows the pad 12 under the metal layer 102; as such it is one of ordinary skill in the art would recognize that figure 14A would also include the pad under the metal layer) is formed and a second surface (bottom surface) opposite to the first surface, the chip component 10b being mounted in such a manner that the second surface faces the substrate 84;

- a metal layer 102 formed on the pad;
- an insulating section 104b/104c formed adjacent to the chip component 10b, the insulating section having an inclined surface descending in an outward direction from the chip component, the inclined surface being a convex surface that draws a curve on a view from which a cross section perpendicular to the first surface of the chip component is taken (figure 14a shows a view from a cross section perpendicular to the first surface of the chip component, as seen in figure 14a the insulating section has an inclined surface that is convex and draws a curve, this section is shown in figure 14a reproduced below); and
- an interconnect 106b which is formed to extend from above the top of the metal layer 102, over the insulating section 104b/104c and to above the interconnect pattern 100, the interconnect covering all the lateral surfaces of the metal layer.



Nakanishi does not explicitly teach the metal layer formed of a plurality of layers including a diffusion prevention layer in contact with the pad and an uppermost layer being less oxidizable than the pad, the diffusion preventing layer preventing any diffusion of material formed thereabove into the base material of the chip component.

Ling et al. teach a chip component 10 of a base material having a first surface on which a pad 26 is formed and metal layer 32/34/36 formed of a plurality of layers including a diffusion prevention layer 32/34 in contact with the pad and an uppermost layer 36 being less oxidizable than the pad, the diffusion prevention layer preventing any diffusion of material formed thereabove into the base material of the chip component.

Nakanishi and Ling et al. are from the same field of endeavor. At the time of the invention, it would have been obvious to one of ordinary skill in the art to form the metal

layer 32/34/36 of a plurality of layers by the method taught by Ling et al. on the pad 12 of Nakanishi. The motivation for doing so is to allow the use of copper interconnect metallization while facilitating the electrical coupling of connection pads to supporting substrates or other packaging while using known metal deposition processes in a simple and inexpensive manner that is compatible with gold bond wires, solder bumps, and other common circuit connection methods and that allows tight spacings between adjacent connections pads without compromising the reliability of the integrated circuit.

With regard to claim 3, Nakanishi does not teach a passivation layer on the first surface of the chip component. However, Ling et al. teaches a passivation layer 13 over the chip where the metal layers (electrode) are exposed through the passivation layer. At the time of the invention it would have been obvious to one of ordinary skill in the art to form a passivation layer over the chip. The reasons for forming a passivation layer are well known in the art, including to passivate and protect the surface of the layers of the chip. In combination, the insulating section has a portion on the passivation layer since the insulating section of Nakanishi covers the chip surface.

With regard to claim 4, Nakanishi further teaches a connecting layer 104b (the portion formed underneath chip 10b) disposed between the chip component and the substrate, wherein the insulating section is formed of the same material as the connecting layer.

With regard to claim 5, Nakanishi as combined with Ling et al. above render the method recited obvious as they perform the claimed "mounting" and "forming" steps as claimed to arrive at the same device of claim 1.

With regard to claim 11, this claim is rejected in the same manner as claim 3 above.

With regard to claim 12, this claim is rejected in the same manner as claim 4 above.

With regard to claim 17, Nakanishi teaches a circuit board (unlabeled bottom cross-hatched portion in figure 10B) on which the device of claim 1 is mounted.

With regard to claim 18, the device of Nakanashi is considered an electronic instrument.

5. Claims 6 and 7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nakanishi with Ling et al. as applied to claims 1, 3-5, 11, 12, 17 and 18 above, and further in view of Ito et al. (US Patent No. 6,625,032 B1).

With regard to claims 6 and 7, Nakanishi does not explicitly teach the interconnect being formed of a dispersant including electrically conductive particles or forming the layer includes ejecting the material over the metal layer, the insulating section, and the interconnect pattern. Nakanishi teach the interconnect being conductive ink but does not explicitly teach a "dispersant including electrically conductive particles."

Ito et al. teach on column 1 lines 30-37 that a dispersant including electrically conductive particles is ejected onto a substrate to form conductive layers. It would have been obvious to one of ordinary skill in the art at the time of the invention to use the

prior art conductive particles in dispersant ejecting method of Ito et al. in the method of Nakanishi to obtain rapid implementation of interconnects on surfaces.

6. Claims 2 and 8-10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nakanishi with Ling et al. or Nakanishi with Ling et al. with Ito et al. as applied to claims 1, 3-7, 11-12, 17 and 18 above, and further in view of JP 01-164044.

With regard to claims 2 and 8-10, Nakanishi does not teach the insulating section being formed of a resin. Nakanishi teach the insulating section 104 being formed of any suitable non-conducting material with can be applied to the die, such as epoxy or polyimide (see column 5 lines 45-47). Nakanishi teach the insulating section applied over the substrate 84 and along the side of the chip 10 to surround the chip. JP 01-164044 teach forming an insulating section in a configuration similar to that of Nakanishi in that it is formed on the substrate 1 and along the side of the chip 4 to surround the chip. JP 01-164044 teach the insulating section being formed of resin. At the time of the invention it would have been obvious to one of ordinary skill in the art to employ a resin as taught by JP 01-164044 for the insulating section 104 of Nakanishi. Nakanishi teaches that any suitable non-conducting material can be used and JP 01-164044 merely teaches one example of a suitable material (resin) used in the same manner as Nakanishi. It has been held that the use of conventional materials to perform their known functions in a conventional process is obvious. *In Re Raner* 134 USPQ 343 (CCPA 1962). Further, it has been held to be within the general skill of a worker in the

art to select a known material on the basis of its suitability for the intended use as a matter of obvious design choice. *In Re Leshin,* 15 USPQ 416.

Double Patenting

7. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. A nonstatutory obviousness-type double patenting rejection is appropriate where the conflicting claims are not identical, but at least one examined application claim is not patentably distinct from the reference claim(s) because the examined application claim is either anticipated by, or would have been obvious over, the reference claim(s). See, e.g., *In re Berg*, 140 F.3d 1428, 46 USPQ2d 1226 (Fed. Cir. 1998); *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) or 1.321(d) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent either is shown to be commonly owned with this application, or claims an invention made as a result of activities undertaken within the scope of a joint research agreement.

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

8. Claims 1-12, 17 and 18 are provisionally rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claims 1-34 of copending Application No. 10/788449 in view of Nakanishi and Ling et al. Claims 1-34 contain all the limitations of claims 1-18 except for a metal layer on the pad where the metal layer is a plurality of layers as claimed, the insulating section having an inclined surface as claimed, and the interconnect pattern covering all the lateral surfaces of the metal layer. However, the plurality of metal layers as claimed is obvious in view of Ling et al. for the same reasons as explained above. The insulating section having an inclined surface as claimed is obvious in view of Nakanishi which teaches an incline in the insulator to allow for a plane with no steep stepped part so that a low cost interconnection method such as screen printing can be used. The inclined surface of the insulating section of Nakanishi reads on the inclined surface as claimed.

This is a provisional obviousness-type double patenting rejection.

Response to Arguments

9. Applicant's arguments filed 12/4/06 have been fully considered but they are not persuasive.

Applicant has argued that Nakanishi fails to teach the inclined surface is a convex surface that draws a curve on a view which is taken from a cross section perpendicular to the first surface of the chip component. This is not persuasive. As explained in the rejection above, the inclined surface that bulges slightly outward (as recognized by applicant in line 12 of page 7 of their response) is a convex surface. The view shown in the figure is taken from a cross section perpendicular to the first surface of the chip component. Thus, the insulating section of Nakanishi reads on that claimed. Applicant further argues that insulating layers 104a, 104b located above substrate contacts 100 (seemingly the same section that forms the convex surface) are not positioned at a location that is at a cross section perpendicular to the upper surface of the die. This is not persuasive. The entire figure 14a is a cross section perpendicular to the upper surface of the die. The claim does not limit the convex surface as being in any particular part of the cross section, or the cross section itself only being a cross section of the area of the chip alone, but rather the claim recites a view from the cross section. Since figure 14a is just such a view, the convex surface shown therein reads on the convex surface claimed.

Conclusion

10. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to N. Drew Richards whose telephone number is (571) 272-1736. The examiner can normally be reached on Monday-Friday 9:00-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ken Parker can be reached on (571) 272-2298. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

N. DREW RICHARDS
PRIMARY EXAMINER